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Novel gate dielectrics for nanoscale semiconductor devices

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Abstract : With the gate length of MOS devices decreasing to <100 nm, scaling requires ultra-thin dielectric layers which provides a challenge to existing technology. Thermally-grown amorphous SiO_2 has been the industry standard because of its high stability, excellent interface quality and electrical isolation properties. However as the gate length shrinks below 70 nm, the SiO_2 (κ = 3.9) thickness required becomes less than 1.5 nm. This leads to unacceptable increase in leakage current density to ~1 A/cm² at 1 V. One remedy is the use of high κ gate dielectrics (κ > 10) which will permit the use of thicker layers for the same capacitance/area. The choice of an appropriate dielectric involves (a) fundamental material properties such as stability with required semiconductor, high permittivity and barrier height and (b) good interface quality, compatibility with existing device processing, integration and reliability.

This paper describes the work carried out with oxides of Gd, Y and Ga as gate dielectrics on SiGe. The MIS structures were formed by evaporation and characterized by I-V, C-V, G-V and SIMS measurements. It was found that though Gd_2O_3 and Y_2O_3 had the highest resistivity and breakdown strength, GGG ($Gd_3Ga_5O_{12}$) gave the lowest D_{it} of 4.8 × 10¹¹/cm².eV and the lowest fixed oxide charge of 8.4 × 10¹⁰/cm². SIMS studies on GGG/SiGe showed significant amount of GaO and GdO along with Ga and Gd. The depth profile showed a relatively sharp interface at ~20 nm. An MOS structure with EOT of 6.9 nm was realized as an example of a nanoscale device.

Keywords . Rare-earth oxides, gate dielectrics, nanoscale device

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1. Introduction

The continuing and astonishing increase in device density and performance of semiconductor chips is due to the robustness of silicon as an electronic material coupled with the unique properties and compatibility of its oxide SiO_2. The advantages of diminishing size can be summed up by the assessment that a 30% reduction in device dimensions can increase speed by a factor of 2 with doubling the number of dies per wafer at half the cost [1].

Apart from its other excellent properties such as stability and dielectric insulation, the ultra-low interface state density (< 10^{10}/cm². eV) of the Si-SiO_2 system makes it difficult to replace in CMOS and other FETs. The defect density in amorphous SiO_2 is also quite small due to its large cohesive energy and the flexibility of the Si-O network. However with the trend to further miniaturization as exemplified by gate lengths being reduced to 70 nm, the thickness of the required oxide approaches 1.5 nm. At this value the current through the dielectric is due to tunneling reaches unacceptably high value of ~1A/cm² at 1 V. Since the gate capacitance for a parallel – plate geometry is given by

$$C = \kappa \varepsilon_0 A / t$$

where κ = relative dielectric constant of gate dielectric, ε_0 = permittivity of free space 8.85 × 10^{-12} F/m, A = area and t = thickness of capacitor, it is evident that an increase in κ will permit an increase in t for the same value of C. Since SiO_2 has κ = 3.9 the gate thickness t_k of high-κ material equivalent to SiO_2 of 'effective oxide thickness' (EOT) t_{eq} can be defined as

$$t_k = (\kappa / 3.9) t_{eq}.$$

Thus for material with κ = 16, a thickness t_k = 4 nm will substitute for oxide thickness t_{eq} = 1 nm. Thus the search is thus on for a high-κ gate dielectric which will provide at least a temporary solution to the problem.

The important parameters of the gate dielectric that must be considered have been discussed by Wallace and Wilk [1]. These are :

(i) permittivity, (ii) band structure and band offsets, (iii) thermodynamic stability, (iv) interface quality, (v) film

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morphology, (vi) gate electrode compatibility, (vii) process compatibility and (viii) reliability. The first 4 factors involving material issues will be discussed here.

To get an idea of the complexity of the problem, it is necessary to realise the actual geometry of the gate stack involved shown in Figure 1. Besides the gate dielectric this involves the gate electrode, the upper interface, the lower interface, channel layer and the Si substrate. Thermodynamic stability thus involves the stability of the entire stack under processing conditions and subsequent performance under load with high reliability.

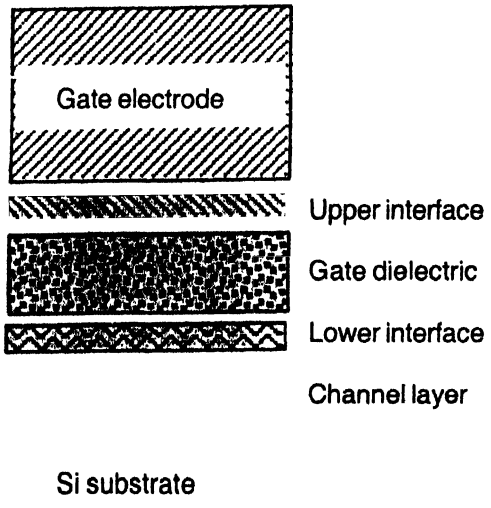

Figure 1. Schematic of gate stack in CMOS FET (after Wallace and Wilks).

2. Thermodynamic stability

Thermodynamic stability of a metal oxide MO with Si can be assessed considering the reaction of an oxide MO (or M_mO_n in general) as

$$Si + MO \quad SiO + M \qquad \Delta G^0_{1000K}$$

or $$Si + MO \quad SiO + MSi \qquad \Delta G^0_{1000K}$$

where ΔG^0_{1000K} is the Gibbs free energy change in the reaction and is –ve for reactions proceeding towards the right. Schlom and Haeni [2] have made a detailed analysis and shown that Be, Mg, Zr, Al, Ca, Sr, Hf and the rare-earth oxides such as those of Ce, Pr , Nd and Gd satisfy the thermodynamic stability criterion. Oxides such as Ta_2O_5, TiO_2 and (Ba, Sr)TiO_3 have, on the other hand, all been shown to be unstable in contact with Si.

Similar analyses has been carried out for the thermodynamic stability of nitrides MN_x in contact with Si which show that Ti, Zr Al nitrides are stable while B, Be, Hf and W nitrides may be conditionally stable. Some of these nitrides *e.g* TiN are conductors while the others have relatively low dielectric constants in the range of 5–9 compared with 4–24 for the oxides. Thus the oxides are more promising than the nitrides.

The thermodynamic stability criteria are for specific conditions and unwanted reactions can still occur if the processing is carried out in oxidizing or reducing ambients. In the first case O can diffuse through the dielectric and oxidize Si while in the latter case the gate dielectric can be reduced to a product which can react with Si.

3. Dielectric constant, band gap and band offset

High values of the dielectric constant for stable oxides being the object of the search, it is found that there is an approximate inverse relationship between the dielectric constant and optical band gap of binary and mixed oxides as shown in Figure 2. The optical band gap should be preferably >5 eV for satisfactory insulation, which rules out a number of dielectrics. SiO_2 with E_{opt} = 9 eV is exceptionally good while TiO_2 with E_{opt} ~ 3 eV and Ta_2O_5 with ~4.5 eV are not satisfactory from this point of view while MgO, CaO, ZrO_2 , HfO_2 and Y_2O_3 are acceptable.

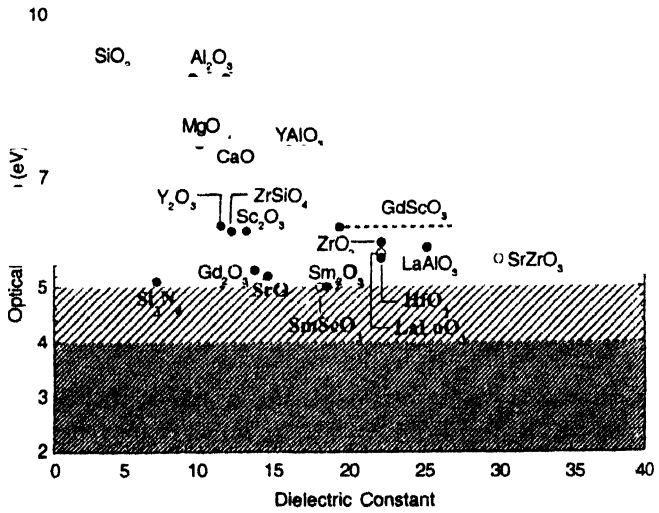

Figure 2. Relationship between the dielectric constant and optical band gap of binary and mixed oxides (after Schlom and Haeni).

Other key parameters are the band offsets ΔE_C and ΔE_V *i.e.* the location of the conduction and valence bands of the oxide with respect to the Si band edges. For low leakage currents, ΔE_C and ΔE_V should be >1 eV. Again SiO_2 with band offsets of 3.5 eV and 4.4 eV is near ideal while $BaTiO_3$ and Ta_2O_5 are deficient in this respect. Among stable oxides ZrO_2 has offsets of 1.4 eV and 3.3 eV while HfO_2 has 1.5 eV and 3.4 eV respectively [3]. It is interesting to note that the stability and the band offset requirements choose the same oxides with high metal *d* states which yield high formation energies.

4. Experimental

With the above considerations in mind it was decided to carry out a systematic study of the oxides of Gd, Y and Ga *viz.* Gd_2O_3,

Y_2O_3 and Ga_2O_3 as gate dielectrics on strained $Si_{0.74}Ge_{0.26}$ (E_{ci} = 0.95 eV). This material has the advantage of enhanced hole mobility over Si and has been shown to be fully compatible with advanced Si technology for heterostructure complementary metal-oxide-semiconductor (CMOS) devices [4]. It is assumed here that with 26% Ge, the same thermodynamic criteria as for Si are valid for $Si_{0.74}Ge_{0.26}$. The deposited films were characterized by EDAX, SIMS, G-V, C-V and I-V measurements. The properties of these and some other oxides are given in Table 1.

Table 1. Properties of some oxides as gate dielectrics on silicon.

Oxide	Band gap (eV)	Dielectric constant	C. band offset ΔE_C (eV)	V. band offset ΔE_V (eV)
Gd_2O_3	5.3	13.6		
Y_2O_3	6.1	16	2.3	2.6
Ga_2O_3	4.4	10		
ZrO_2	5.8	22	1.4	3.3
HfO_2	5.5	21	1.4	3 4
La_2O_3	5 7	25–30	2.3	2.6
Al_2O_3	8.7	11	2.8	4.9

It may be mentioned that GGG/GaAs interfaces prepared in ultra high vacuum have been reported to have low interface state densities and have resulted in GaAs n- and p-MOS devices [5]. Conventional thermal oxidation for the growth of gate oxide on strained SiGe causes strain relaxation and Ge segregation at the oxide-semiconductor interface [6]. Epitaxial layers of strained $Si_{0.74}Ge_{0.26}$ 30 nm thick was grown by ultra high vacuum chemical vapour deposition on a Si buffer layer 50 nm thick at 550° C on (100) p-Si substrates using SiH_4 and GeH_4. The layers were B doped *in situ* at (1–2) × 10^{17}/cm^3. The samples were RCA cleaned followed by cleaning with 1: 1 H_2SO_4 and H_2O_2 solution. Finally the native oxides from the samples were removed using dilute HF solution prior to insulator deposition.

Dielectric films of different thicknesses (20–350 nm) were deposited by electron-beam evaporation at room temperature at a pressure of 3 × 10^{-6} torr [7]. Single crystal $Gd_3Ga_5O_{12}$ was used as the source of $Ga_2O_3(Gd_2O_3)$ film whereas powder-packed high purity Ga_2O_3, Gd_2O_3 and Y_2O_3 sources were used for electron-beam evaporation of respective oxide films. Since e-beam evaporated oxide films are usually oxygen deficient, the deposited films were subjected to a post-deposition anneal at 450°C in oxygen atmosphere for 10 min. A higher temperature anneal was avoided to prevent the strain relaxation of the SiGe epilayer. The composition of the $Ga_2O_3(Gd_2O_3)$ film was determined using energy dispersion analysis of X-ray (EDAX) spectroscopy using a scanning electron microscope (JSM 5800). The thickness and refractive indices of the films were measured by a single-wavelength (λ = 638 nm) Gaertner L 117 ellipsometer.

The GGG/SiGe structures were characterized by Secondary Ion Mass Spectrometry (SIMS) for the top layer composition and presence of surface impurities in the survey scan mode. SIMS was also used in depth profile mode to study the oxides and interfaces. Cs^+ ions were used as a primary beam of 11 KeV energy with beam current of 40–60 nA. Depth calibration was carried out using a Tencore Alpha step 500 surface profilometer of the craters after SIMS depth profiling.

MOS structures were fabricated by depositing Au electrodes of area 2.8 × 10^{-3} cm^2 through a metal mask by thermal evaporation. Evaporated Al was used as the back contact on SiGe. The fixed insulator charge and interface state densities were determined from the conductance-voltage (G-V) and capacitance-voltage (C-V) characteristic using a HP 4061A semiconductor test system and a HP 4145B parameter analyzer. The resistivity and dc breakdown field of the films were studied using the I-V characteristics.

5. Results and discussion

The composition of the deposited GGG films was determined quantitatively by Energy Dispersion Analysis (EDAX). The concentration ratio of Ga_2O_3 : Gd_2O_3 was thus found to be 98.4 % : 1.6%. Thus the film was found to be non-stoichiometric mainly consisting of Ga_2O_3. This is due to the relatively high vapour pressure of Ga_2O_3.

The SIMS survey scan of the $Ga_2O_3(Gd_2O_3)$/SiGe sample (Figure 3) showed appreciable signals from Ga and Gd along with GdO. The depth profiles taken for O, Si, SiO, Ga, Ge, Gd and GdO showed a sharp interface at a depth of 20 nm. The presence of a thin SiO_2 layer at the interface was indicated. The variation of Ga concentration through the film is found to follow that of the O concentration. Ge pile-up at the interface that occurs on thermal oxidation is notably absent.

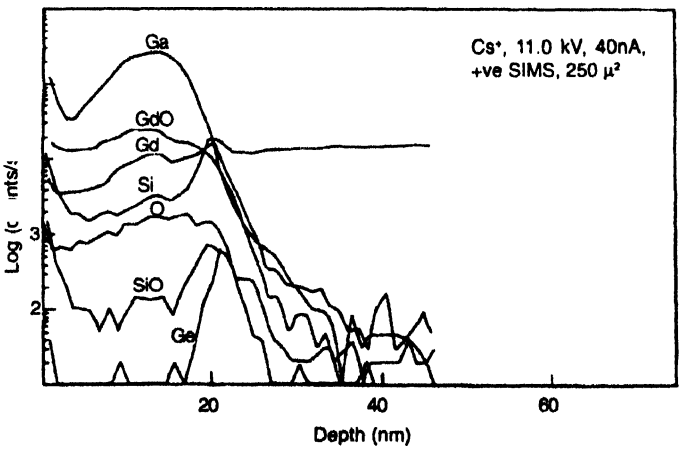

Figure 3. SIMS depth profile of a 20 nm $Ga_2O_3(Gd_2O_3)$ film on strained p-$Si_{0.74}Ge_{0.26}$ after annealing.

From the I-V characteristics between 10–300 K, three distinct mechanisms of current conduction through the dielectric films were observed *viz.* tunneling at lowest temperatures, followed

by ohmic conduction and Poole-Frenkel conduction near room temperature (Figure 4). Resistivity values for the different films were derived from the linear region of the I-V characteristics at low fields. On annealing the resistivity increased while the leakage current decreased by one order of magnitude. The current density J *vs* electric field E in the linear region for different films is shown in Figure 5. The resistivity, dc breakdown field, leakage current, interface state density and fixed oxide charge density of different oxide films are summarized in Table 1. The Gd_2O_3 and Y_2O_3 films showed the highest resistivity after

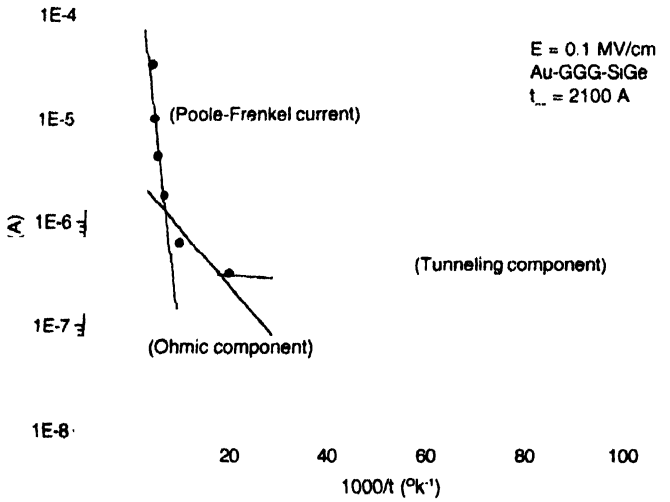

Figure 4. Current (I) *vs* 1000/T plot for an $Au/Ga_2O_3(Gd_2O_3)/Si_{0.74}Ge_{0.26}$ MOS capacitor showing 3 conduction mechanisms.

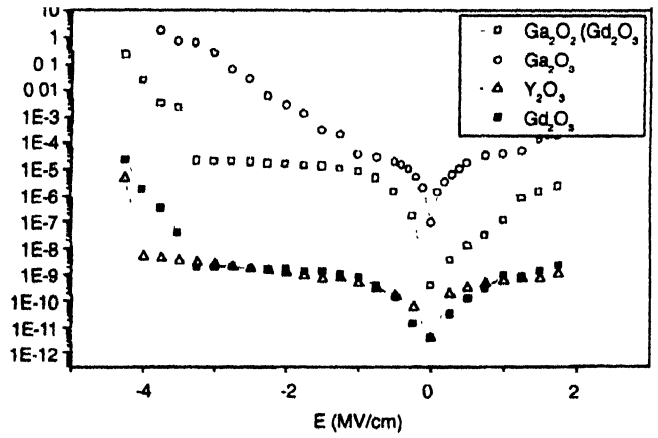

Figure 5. Reverse current density J_R *vs* voltage for different oxide films on $Si_{0.74}Ge_{0.26}$ after annealing.

annealing (~10^{14} Ω. cm), lowest leakage current density (< 10^{-11} /A.cm^2) and highest breakdown field of (~ 4 MV/cm). The Ga_2O_3 film on the other hand showed the lowest resistivity and breakdown voltage and the highest leakage current. This is due its lowest band gap of 4.4 eV which makes for low band offsets. Further high defective density is indicated which also leads to a very low breakdown voltage.

The static dielectric constants given in Table 2 are derived from the accumulation regions of the C-V characteristics (1

Table 2. Comparison of properties of different gate oxides.

Dielectric film	Ga_2O_3	$Ga_2O_3(Gd_2O_3)$	Gd_2O_3	Y_2O_3
Thickness (nm)	197.5	208.8	205.6	206.3
Dielectric constant (ε_r)	10.0	12.3	13.6	16.0
Resistivity ρ (Ω.cm)	1.6×10^{10}	6.1×10^{12}	1×10^{14}	6.8×10^{11}
Reverse saturation current I_R (A)	1×10^{-7}	5.2×10^{-8}	1×10^{-11}	1×10^{-11}
Breakdown field E_B (MV/cm)	1.0	3.25	3.28	4.01
Interface state density D_{it} (eV^{-1} cm^{-2})	2.4×10^{12}	4.9×10^{11}	6.29×10^{11}	5.4×10^{11}

MHz) shown in Figure 6. The curve for the Ga_2O_3/SiGe interface is found to be strikingly different from the others in being stretched out indicating its inability to passivate the SiGe surface. The $Ga_2O_3(Gd_2O_3)$ film shows the sharpest C-V curve indicative of lowest interface state densities.

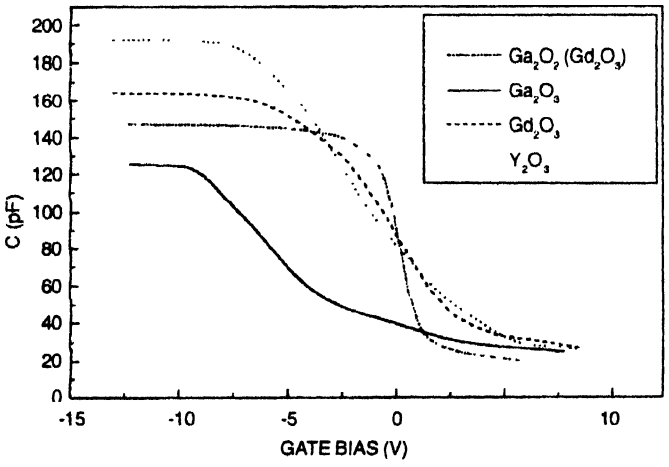

Figure 6. C–V characteristic (1 MHz) of oxide – $Si_{0.74}Ge_{0.26}$ MOS devices

Figure 7 shows the G-V curves at 100 KHz for all the films. The Ga_2O_3/SiGe sample shows poor properties with the highest conductance and largest stretch-out. The $Ga_2O_3(Gd_2O_3)$/SiGe interface shows the lowest conductance with sharpest variation while the other 2 films show intermediate behaviour. The interface state densities D_{it} (eV^{-1}.cm^{-2}) derived from the G-V characteristic using Hill's method [8] are thus lowest for the $Ga_2O_3(Gd_2O_3)$/SiGe interface as given in Table 2. Correction for series resistance is incorporated into the calculation. It is interesting to note that while the Ga_2O_3 films show the poorest characteristics, a small addition of 1.54% of Gd_2O_3 increased the resistivity by 2 orders of magnitude, reduced the leakage current and the interface state density significantly. This suggests an important role for Gd which is known to have a +3 oxidation state while Ga can have either +1, +2 or +3 charge states. The presence of a small amount of an electropositive rare-earth element like Gd, it has been suggested, helps stabilize Ga in the +3 state [9]. Thus the high leakage current in Ga_2O_3 may be due to the presence of sub-oxides. The fixed oxide charge, also found

in each case, was the lowest for GGG (8.4×10^{10} /cm^2) [7] and decreased on annealing.

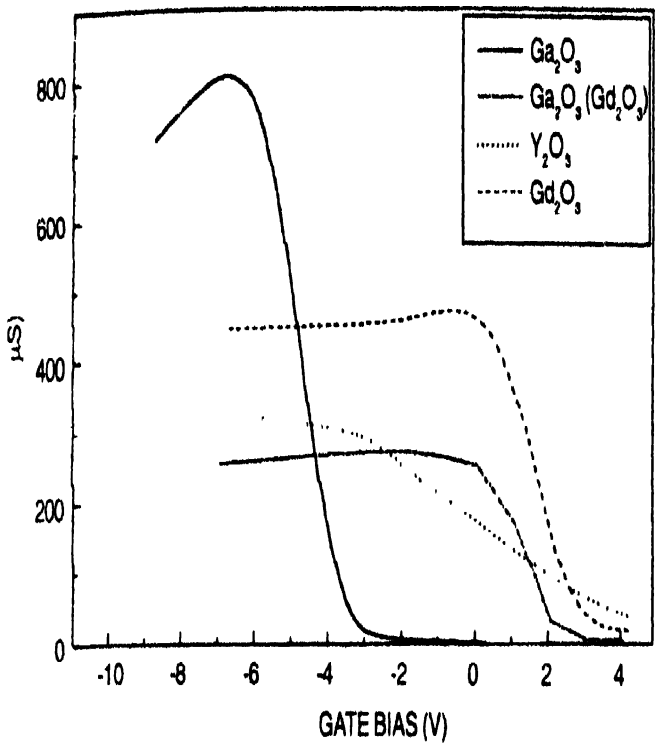

Figure 7. G-V characteristic (100 KHz) of oxide – $Si_{0.74}Ge_{0.26}$ MOS devices

The minimum value of D_{it} is found to be 4.9×10^{11} /eV.cm^2 for the $Ga_2O_3(Gd_2O_3)$/SiGe interface which is equal to the best reported for high-k dielectrics on SiGe [10]. The thickness of the $Ga_2O_3(Gd_2O_3)$ film was reduced to 20 nm and the electrical characteristics found to be of the same high quality. Thus this device represented a MOS capacitor with equivalent oxide thickness (EOT) of 6.9 nm.

6. Conclusions

This study on rare-earth oxides as gate dielectrics showed that of the materials studied (GGG) $Ga_2O_3(Gd_2O_3)$ yielded the best properties on strained p–$Si_{0.74}Ge_{0.26}$ with lowest interface state density D_{it}. This is similar to the results of GGG/ GaAs reported by Passlack *et al* [5]. Comparison with Ga_2O_3 showed that the role played by 1.54% Gd_2O_3 was crucial in improving the properties. An MOS structure on SiGe with EOT of 6.9 nm was realized as an example of a nanoscale device.

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